

Appl. No. : 10/021,388
Filed : December 6, 2001

REMARKS

In response to the Office Action, Applicant respectfully requests the Examiner to reconsider the above-captioned application in view of the foregoing amendments and the following comments.

Discussion of Claim Rejections Under 35 U.S.C. §§ 102(e) and 103(a)

In the Office Action, the Examiner rejected Claims 2-7 and 9-11 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,764,590 to Iwamoto (hereinafter "Iwamoto"). The Examiner rejected Claims 1 and 8 under 35 U.S.C. § 103(a) as being unpatentable over Iwamoto in view of U.S. Patent No. 5,537,584 to Miyai, et al (hereinafter "Miyai").

One embodiment of Applicant's invention includes a switch that is used to control the parasitic capacitance of a bus. Claim 1 recites: "wherein the switch is operated so as to control the parasitic capacitance of the input/output terminals." Independent Claims 2, 4, 7-9, and 11 recite similar limitations.

Applicant respectfully submits that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference. *See* M.P.E.P. § 2131. Furthermore, to establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *See* M.P.E.P. § 2143.03. Applicant respectfully submits that the cited references fails to teach or suggest at least one limitation from independent Claims 1, 2, 4, 7-9 and 11.

Iwamoto describes a selector (904). The selector (904) routes signals from a input buffer to one of two write registers. *See* Iwamoto, col. 11, line 50 - col. 12. line 3. Applicant respectfully submits that there is no teaching or suggestion in Iwamoto that the selector (904) is used to control the parasitic capacitance of a bus. The selector (904) merely acts as a router of information. It does not control parasitic capacitance, such as by example, electrically isolating portions of a bus. Applicant respectfully submits that a selector does not inherently perform the function of electrically isolating portions of a bus. The input selector (904) is merely used to functionally activate a signal to either an input buffer A or an input buffer B. Figure 11 illustrates a specific configuration of an input selector (904). The input selector (904) is comprised of inverters (1101 and 1102). There is no teaching or suggestion that inverters (1101

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and 1102) serve the purpose of controlling the parasitic capacitance of either the input buffer A or the input buffer B.

“In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to support the determination that the inherent characteristic necessarily flows from the teachings of the applied prior art.” See M.P.E.P. § 2112. Applicant respectfully submits that the selector (904) need not necessarily electrically control the parasitic capacitance. The use of a selector having inverters does not necessarily mean that the selector electrically isolates portions of a bus. Thus, Applicant respectfully submits that since Iwamoto does not teach or suggest each and every element of Claims 2, 7, 9, and 11, these claims are not anticipated and are in condition for allowance.

Furthermore, Applicant respectfully submits that these features are not taught or suggested by Miyai. Miyai was cited by the Examiner in support of the proposition that chip select signals were well known in the art. Applicant respectfully submits that Miyai fails to teach or suggest the use of a chip select signal so as to control the parasitic capacitance of a bus. In the Office Action, the Examiner stated that in independent Claims 1 and 8, the control of the parasitic capacitance is independent of the chip select signal. Applicant respectfully submits that these claims have been amended to clarify this issue. Furthermore, in the Office Action, the examiner stated the usage of the word “wherein” is inappropriate. Although Applicant disagrees, he has amended the claims as relating to remove reference to the word “wherein” with respect to the operation of controlling the parasitic capacitance. Furthermore, Applicant has amended the claims to further clarify the type of switch that is being used, i.e., a parasitic capacitance control switch.

Since Iwamoto and Miyai fails to teach or suggest at least the above limitation in isolation or in combination, Applicant respectfully submits that independent Claims 2, 4, 7-9, and 11 are in condition for allowance. Furthermore, since Claims 3, 5, and 10 each depend on one of Claims 2, 4, and 9, Applicant respectfully submits that these claims are allowable fore the reasons previously discussed.

Summary

Applicant has endeavored to address all of the Examiner’s concerns as expressed in the outstanding Office Action. Accordingly, amendments to the claims for patentability purposes, the reasons therefore, and arguments in support of the patentability of the pending claim set are

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presented above. Any claim amendments which are not specifically discussed in the above remarks are not made for patentability purposes, and the claims would satisfy the statutory requirements for patentability without the entry of such amendments. In addition, such amendments do not narrow the scope of the claims. Rather, these amendments have only been made to increase claim readability, to improve grammar, and to reduce the time and effort required of those in the art to clearly understand the scope of the claim language. In light of the above amendments and remarks, reconsideration and withdrawal of the outstanding rejections is specifically requested. If the Examiner has any questions which may be answered by telephone, he is invited to call the undersigned directly.

Respectfully submitted,

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Dated: 1/30/2007

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